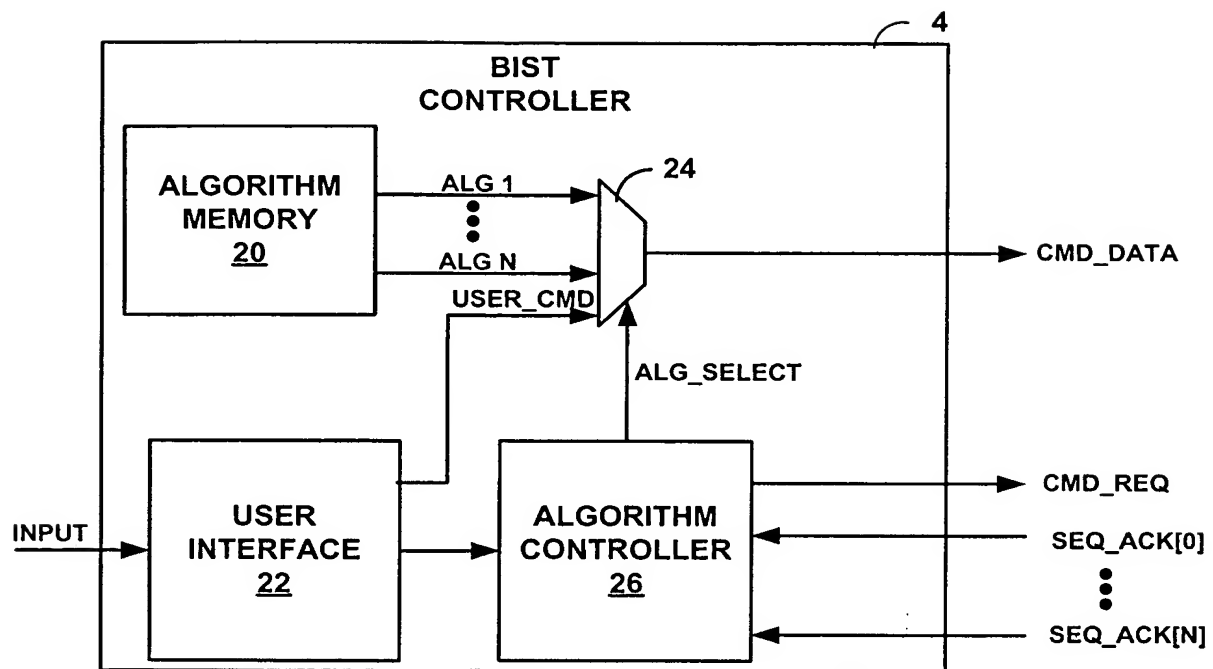


FIG. 1



**FIG. 2**

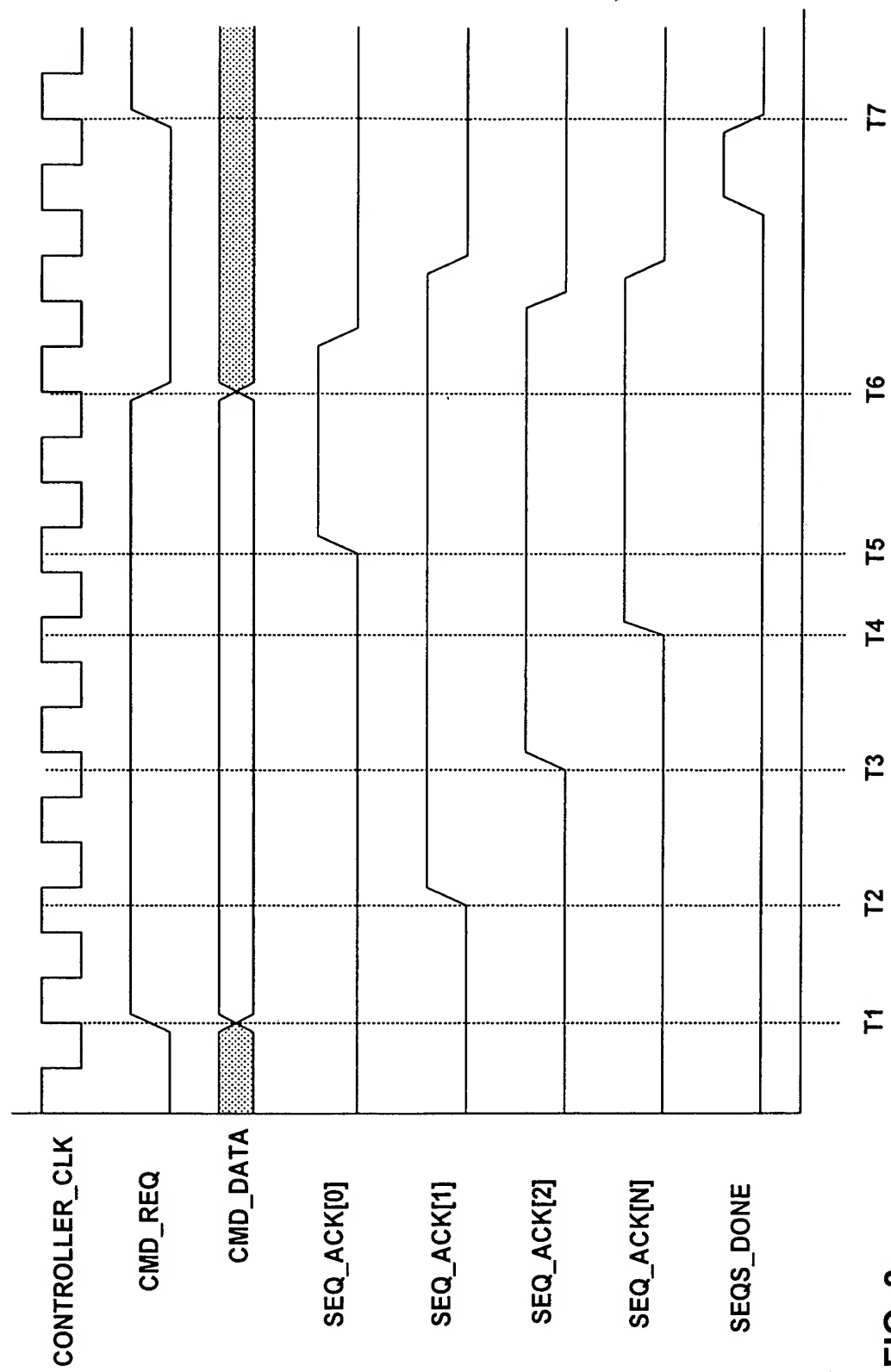
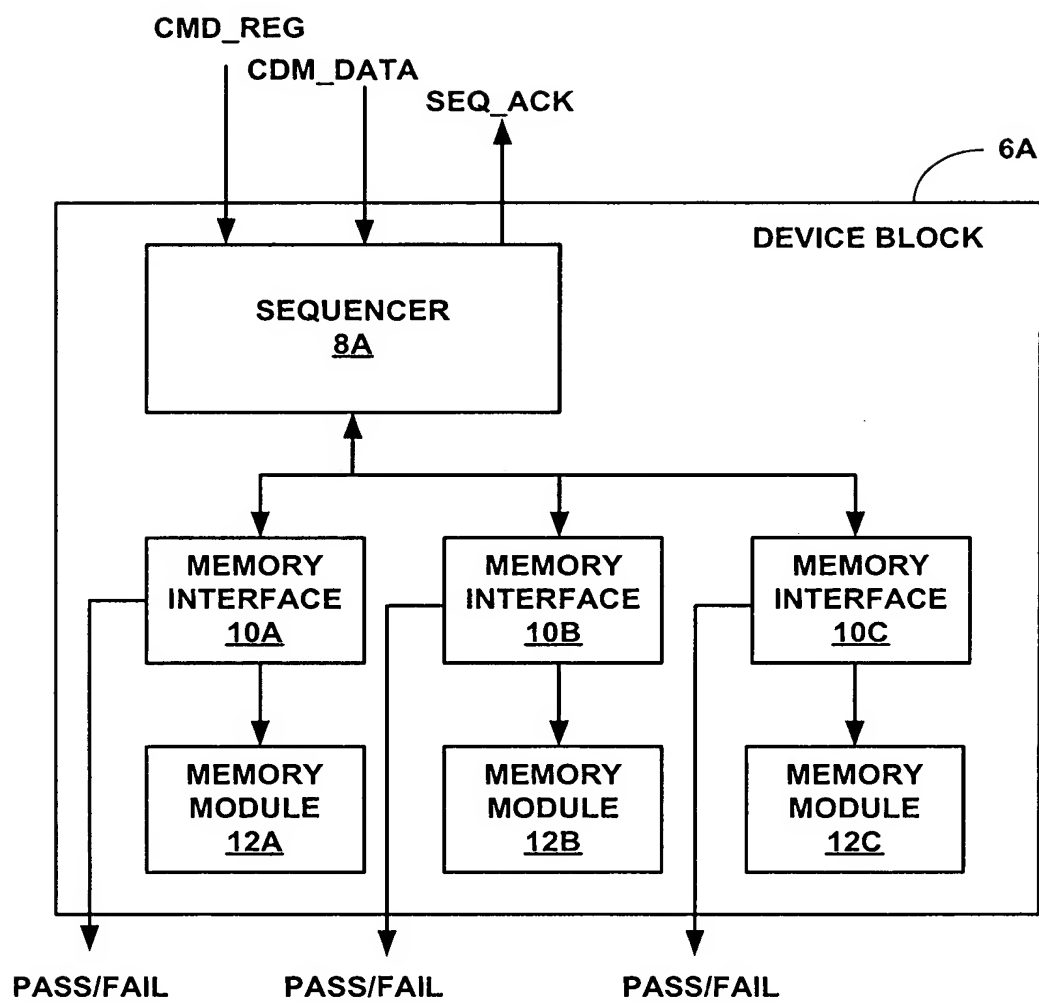


FIG. 3



**FIG. 4**

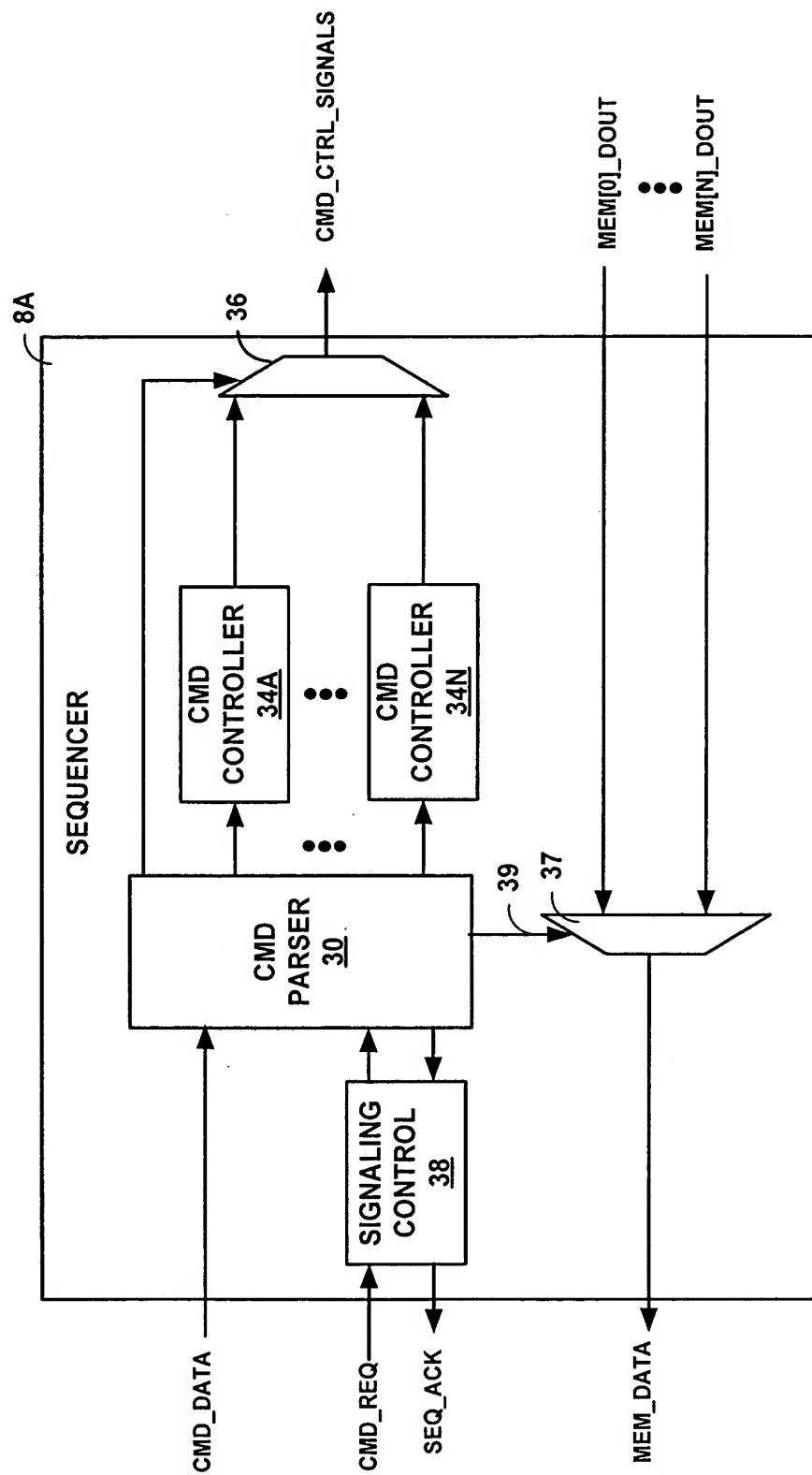


FIG. 5

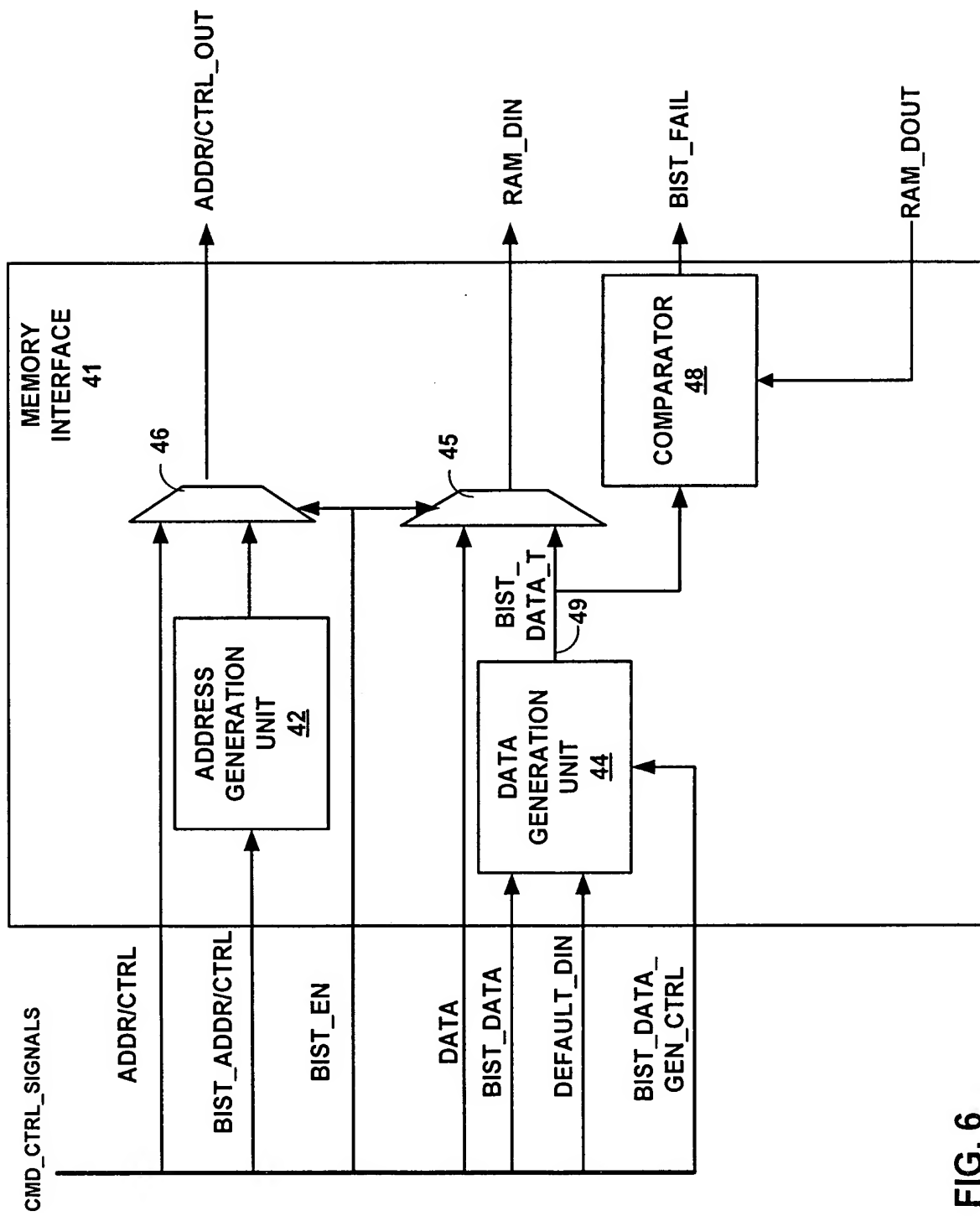


FIG. 6

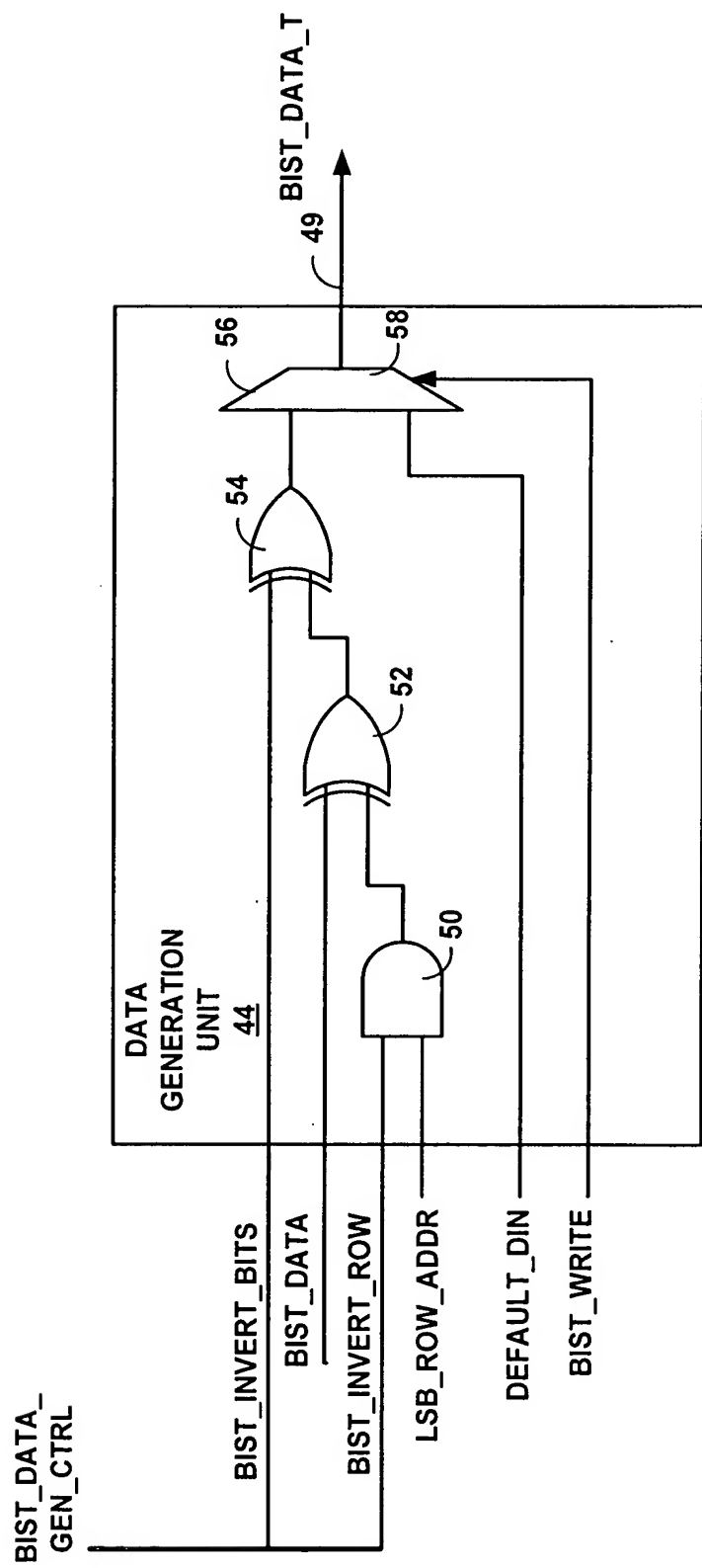


FIG. 7

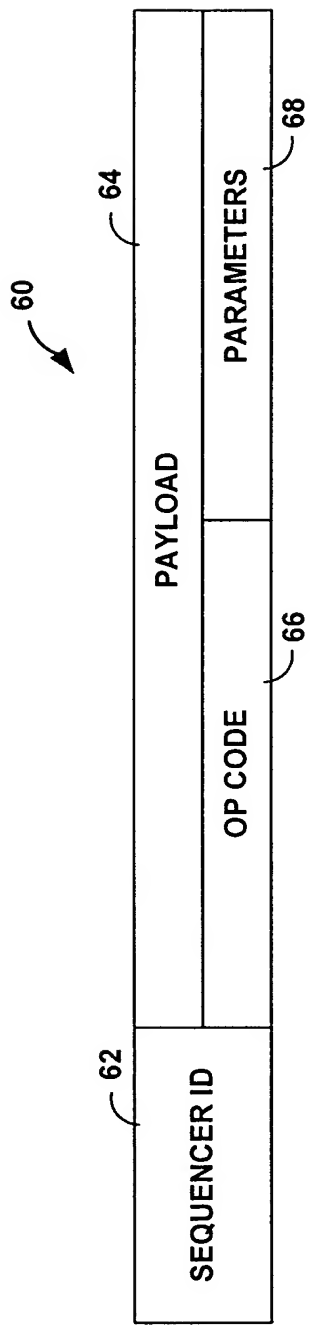


FIG. 8

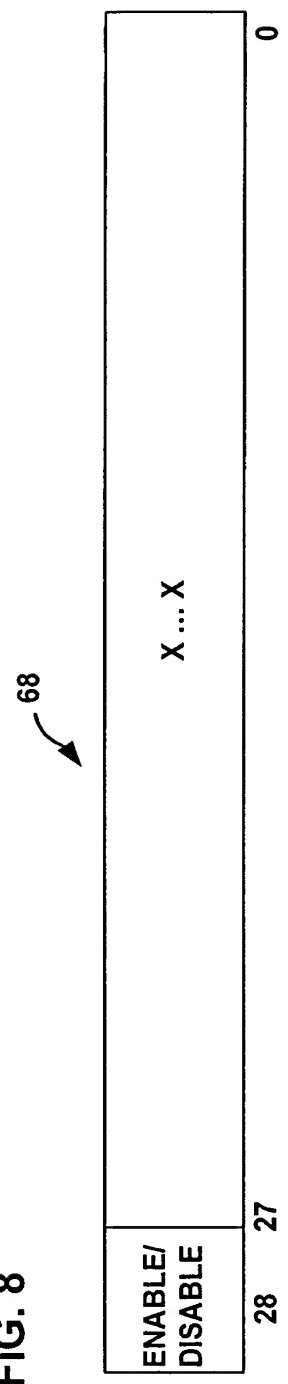


FIG. 9A

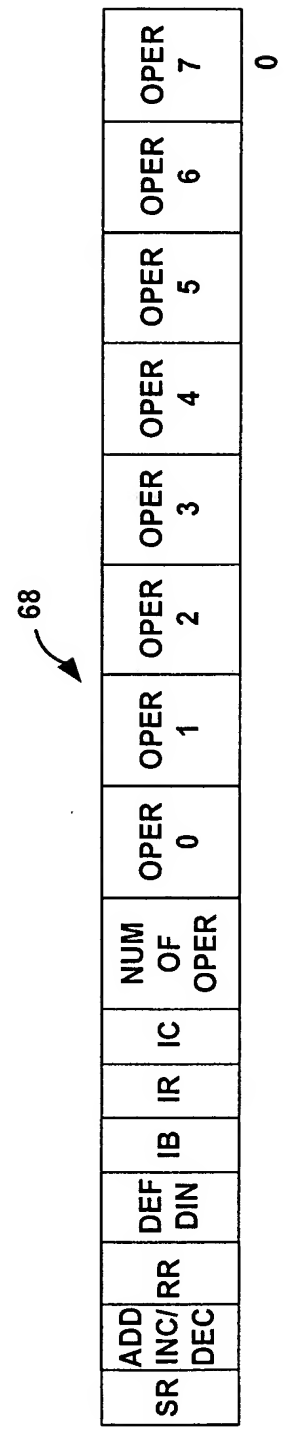


FIG. 9B



68

FA/BIST	ENA / DIS	MEM BUS SLICE	MEM ID
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FIG. 9C

68

LIMIT	ADDRESS
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FIG. 9D

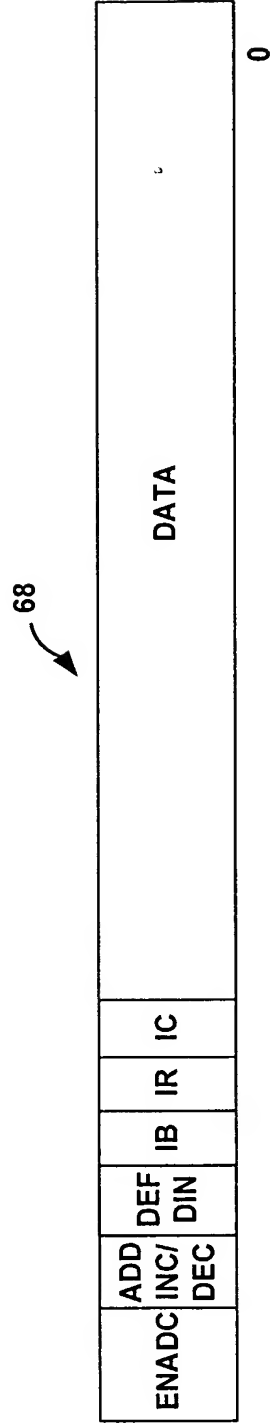


FIG. 9E

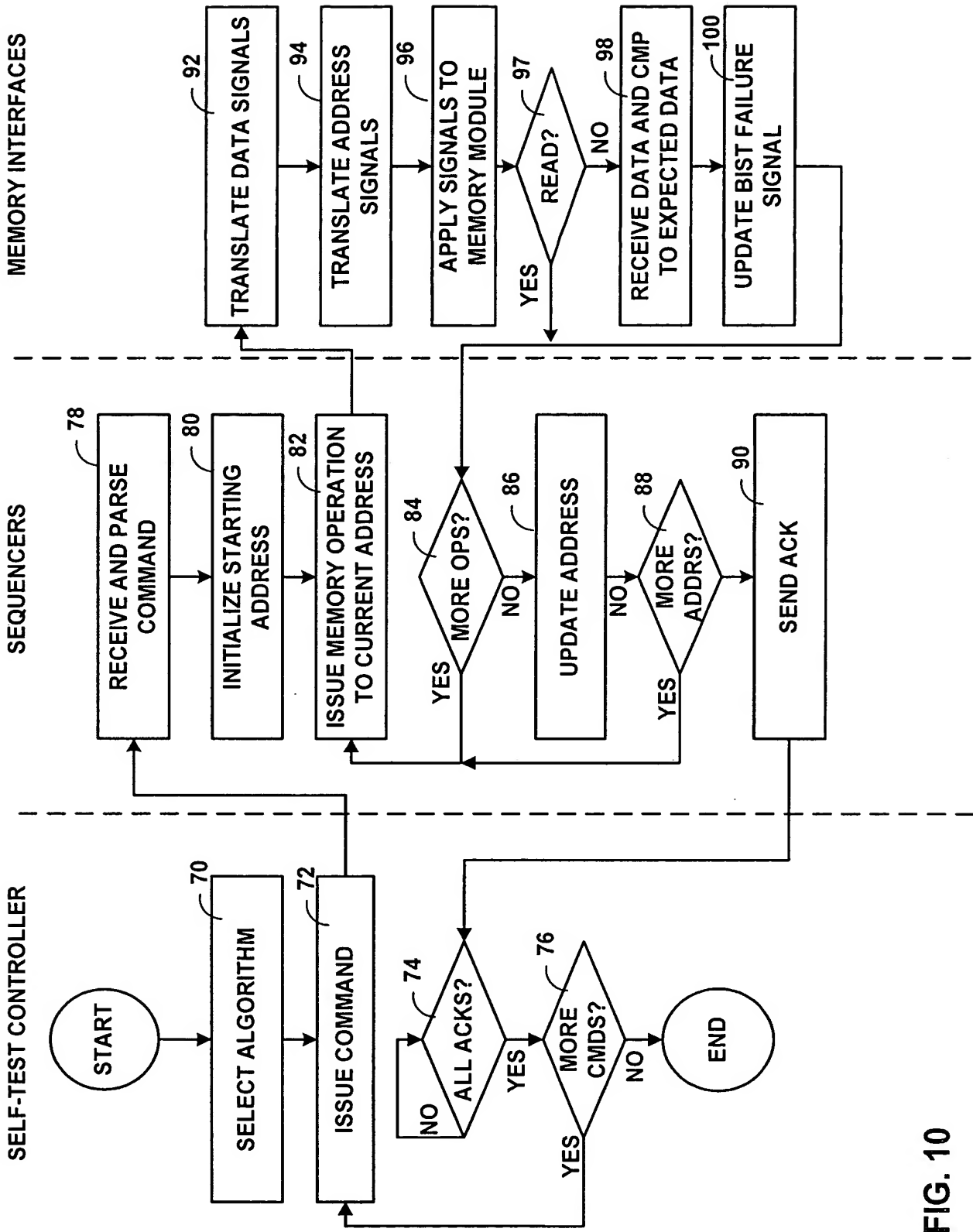


FIG. 10